Analytical Thermal Model for Multilevel VLSI Interconnects Incorporating Via Effect

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***Abstract*—This letter presents compact analytical thermal models for estimating the temperature rise of multilevel VLSI interconnect lines incorporating via effect. The impact of vias has been modeled using 1) a characteristic thermal length and 2) an effective thermal conductivity of ILD (interlayer dielectric), $k_{ILD,eff}$, with $k_{ILD,eff} = k_{ILD}/\eta$, where η is a physical correction factor, with $0 < \eta < 1$. Both the spatial temperature profile along the metal lines and their average temperature rise can be easily obtained using these models. The predicted temperature profiles are shown to be in excellent agreement with the three-dimensional (3-D) finite element thermal simulation results. The model is then applied to estimate the temperature rise of densely packed multilevel interconnects. It is shown that for multilevel interconnect arrays, via density along the lines can significantly affect the temperature rise of such interconnect structures.**

***Index Terms*—Heat dissipation, interconnect, Joule heating, low-k dielectrics, thermal conductivity, thermal modeling, via effect, VLSI, wire temperature distribution.**

I. Introduction

RECENT publications have addressed the issue of low-k dielectrics and their impact on interconnect temperature, reliability, and performance [1], [2]. However, the effect of vias, which have much higher thermal conductivity than the dielectrics and can serve as efficient heat dissipation paths, has not been adequately addressed. Consequently, if via effect is ignored, the predicted temperature rise of interconnects can be much higher than those for actual layouts with vias. Recently, we have demonstrated the strong influence of vias on the temperature distribution in metal lines using an electrothermal circuit simulation methodology [3], [4]. However, analytical thermal models are desirable to facilitate quick estimation of temperature rise in order to provide thermal design guidelines for advanced interconnect structures. In this letter, a compact analytical thermal model incorporating via effect is developed and has been applied to estimate the temperature rise of multilevel interconnect structures.

II. Interconnect Thermal Model and Assumptions

Consider a rectangular metal wire of thickness H, width w, length L, resistivity ρ and thermal conductivity k_M, separated from the underlying layer by ILD of thickness t_{ILD} and thermal conductivity k_{ILD}. With x-coordinate set to zero at the middle of the wire, the two ends, $x = \pm L/2$, of the wire are connected to the underlying layer through vias. The temperature at the ends of the wire is assumed to be the same as the underlying layer temperature, T_0, thus $T(\pm L/2) = T_0$. It is further assumed that heat only flows downwards toward the silicon substrate which is usually attached to a heat sink. Under steady state conditions, with uniform root-mean-square current density, j_{rms}, flowing in the wire, the governing heat equation is given by

$$\frac{d^2T}{dx^2} - \frac{T - T_0}{L_H^2} = -\frac{\rho j_{rms}^2}{k_M}, \quad \text{where } L_H = \left[\frac{k_M H t_{ILD}}{k_{ILD}}\left(\frac{1}{s}\right)\right]^{\frac{1}{2}}. \quad (1)$$

Here ρ is assumed to be a constant at the die temperature for a first order approximation, and L_H denotes the thermal characteristic length. Within the range of L_H from the vias, heat generated in the wire will flow through the vias to the underlying layer. Beyond L_H, heat flows through the ILD and the via effect is diminished. Here s is a heat spreading factor that is employed to correct the deviation from one-dimensional (1-D) heat flow between a metal wire and the underlying layer, and is defined as, $s = w_{eff}/w$, where w_{eff} is the effective width of the dielectric through which heat conduction takes place. The spatial temperature distribution along the wire can then be solved as

$$T(x) = T_0 + \Delta T_{Max}\left(1 - \frac{cosh\left(\frac{x}{L_H}\right)}{cosh\left(\frac{L}{2L_H}\right)}\right), \quad \text{for } -\frac{L}{2} \le x \le \frac{L}{2} \quad (2)$$

where $\Delta T_{Max} (= {j_{rms}}^2 \rho {L_H}^2/k_M)$ is the temperature rise in the wire when via effect is ignored.

Effect of variation in ρ with temperature was found to be small for normal operating conditions and is ignored here. Meanwhile, the much less complex expression for L_H could provide more insight for design guidance. A similar derivation that includes the linear temperature dependent resistivity under electromigration test conditions can be found in [5], [6].

It should be noted that the commonly used Bilotti's equation [7] was derived for a single heat (line) source. However, since, in typical IC layouts, there are multiple heat sources due to parallel and orthogonal metal wire arrays, a new expression for s is derived here. For the worst case scenario, all metal wires are assumed to carry the maximum RMS current density and to be

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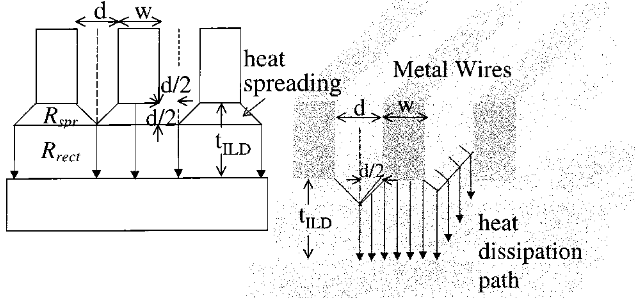

Fig. 1. Geometry used for calculating R_{spr}, R_{rect} and the spreading factor s. Cross-sectional view is shown on the left hand side. Space between any two wires is shared for heat dissipation.

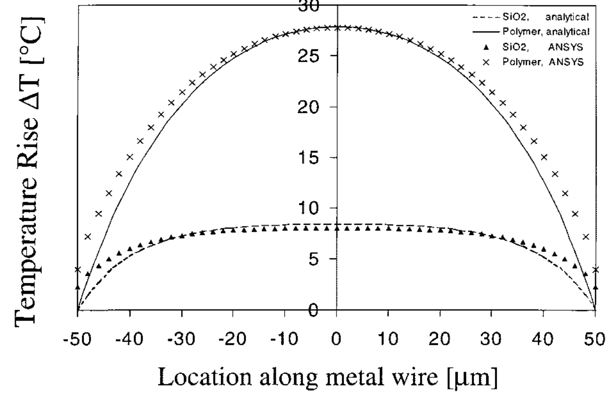

Fig. 2. Temperature profile along the Cu wires with 100 μm via separation. $H = t_{ILD} = 0.8$ μm, $w = d = 0.3$ μm, based on the ITRS [9] 100-nm node for global interconnects. Current density used here is 3.7 MA/cm^2.

separated by spacing d. As shown in Fig. 1, the Joule heat transfers downward and also spreads laterally in the ILD. Hence, the total cross-sectional area through which heat conduction takes place can be divided into two regions whose per unit length thermal resistances are R_{spr} and R_{rect}. Then, the total thermal resistance of ILD , $R_{th,ILD}$, can be calculated by combining R_{spr} and R_{rect} [8] as

$$R_{th,ILD} = \frac{1}{2k_{ILD}} \ln\left(\frac{w+d}{d}\right) + \frac{1}{k_{ILD}} \frac{t_{ILD} - \frac{d}{2}}{w+d}. \quad (3)$$

On the other hand, R_{ILD} can be also expressed as

$$R_{th,ILD} = \frac{t_{ILD}}{k_{ILD} w_{effective}} = \frac{t_{ILD}}{k_{ILD} ws}. \quad (4)$$

By comparing (3) and (4), s, can be obtained as

$$s = \left(\frac{w}{t_{ILD}} \left[\frac{1}{2}\ln\left(\frac{w+d}{w}\right) + \frac{t_{ILD} - \frac{d}{2}}{w+d}\right]\right)^{-1}. \quad (5)$$

After the s factor is installed in the expression for L_H, the effect of the via separation and heat spreading on the temperature profile along a metal wire can be captured completely by (2). As can be observed from Fig. 2, the analytical model given by (2) is shown to be within 5% agreement with the 3-D finite element thermal simulations using ANSYS.

It should be noted that as predicted by the expression for L_H, and validated from Fig. 2, L_H is longer if ILD has lower thermal conductivity. Consequently, via effect is more important for the low-k insulators($k_{polymer} = 0.3$ Vs $k_{oxide} = 1.2$ W/mK). By defining a via correction factor (η), the via effect can be incorporated into the effective thermal conductivity of ILD, $k_{ILD,eff}$, which can then be used in place of the nominal k_{ILD} in the conventional thermal equations. An analytical expression for $k_{ILD,eff}$ incorporating via effect is now derived here. The average temperature rise, ΔT_{ave}, in one metal layer can be expressed as

$$\Delta T_{ave} = q\, R_{th,ILD} = j_{rms}^2\, \rho\, \frac{H\, t_{ILD}}{k_{ILD,eff}\, s} \quad (6)$$

where q is the rate of heat generation. On the other hand, ΔT_{ave} can also be obtained from (2) as

$$\begin{aligned}\Delta T_{ave} =& \frac{1}{L}\int_{-\frac{L}{2}}^{\frac{L}{2}} (T(x) - T_0)dx \\ =& j_{rms}^2 \rho \frac{H t_{ILD}}{k_{ILD} s}\left[1 - \frac{\left(\tanh \frac{L}{2L_H}\right)}{\frac{L}{2L_H}}\right]. \quad (7)\end{aligned}$$

Comparing (6) and (7), we can express $k_{ILD,eff} = k_{ILD}/\eta$ and η is defined as the via correction factor

$$\eta = \frac{k_{ILD}}{k_{ILD,eff}} = 1 - \frac{\left(\tanh \frac{L}{2L_H}\right)}{\frac{L}{2L_H}}, \; 0 \le \eta \le 1. \quad (8)$$

The $k_{ILD,eff}$ is plotted against via separation in Fig. 3 for three different ILD materials. The dimensions of the interconnect structure were taken from the 100-nm technology node for global wires based on the ITRS [9]. It can be observed that incorporation of via effect results in increased $k_{ILD,eff}$ especially for ILD materials with lower nominal thermal conductivity. This can result in a significant difference between the interconnect temperatures obtained with and without considering the effect of the vias.

III. Thermal Model for Multilevel Interconnects

Generally, Joule heat generated in metal wires is considered to be dissipated mainly through the heat sink attached to the underlying Si substrate. Therefore, all the heat generated in the upper metal levels has to transfer through the lower metal levels before reaching the substrate. With $\Delta T_{i-1,i}$ defined as the average temperature rise between metal layers $i-1$ and i, the temperature rise of the top layer in an N-level interconnect system can be obtained as

$$\begin{aligned}\Delta T_N =& T_N - T_{substrate} = \sum_{i=1}^{N} \Delta T_{i-1,i} = \sum_{i=1}^{N} q_i\, R_{th,i} \\ \cong& \sum_{i=1}^{N} \frac{t_{ILD,i}}{k_{ILD,i}\, s_i}\, \eta_i \sum_{j=i}^{N} j_{rms,j}^2\, \rho\, H_j. \quad (9)\end{aligned}$$

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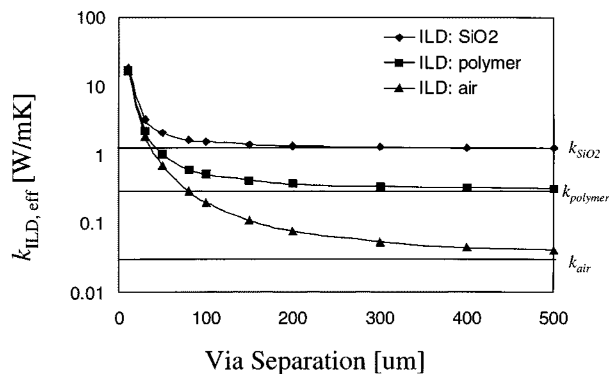

Fig. 3. Effective ILD thermal conductivity increases with decreasing via separation. The lower the nominal k_{ILD}, the longer the L_H, and hence, the stronger is the via effect.

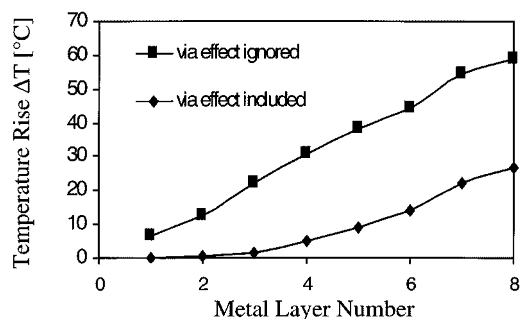

Fig. 4. Distribution of temperature rise along metal layers from metal one to the top metal layer. For the case that includes the via effect, the via separations are 1, 5, 15, 30, 50, 100, 250, and 500 μm, for metal one through metal 8, respectively.

This is a closed form analytical equation that can be used to compute the temperature rise of interconnects in a multilevel interconnect system. For the case when via effect is neglected, η_i is set to be 1.

As can be seen from (9), more heat flows through the lower levels since q_i represents the sum of all the heat generated from the ith layer to the Nth layer. As a result, substantial temperature rise will occur in local wires if the effect of the via population, which is usually dense, is not taken into account. For the purpose of demonstration of the importance of the via effect, some reasonable values of via separation were assigned to each of the eight metal layers and a polymer was used as the ILD material for the 100-nm technology node. In addition, an ITRS based current density, j_{rms}, of 1.4 MA/cm^2 was assumed for all the wires. It can be observed from Fig. 4 that the overall temperature rise is much lower if effect of the vias is included. Secondly, it can be observed that the temperature distribution among metal layers is quite different for these two cases. Ignoring via effect results in large temperature rise in the lower layers before leveling off. On the other hand, with via effect considered, the temperature rise in the lower levels is significantly lower even when the ILD material's nominal thermal conductivity is approximately one fourth of k_{oxide}. Most of the temperature rise is attributed to the upper metal layers with long via separation. Therefore, from the thermal design point of view, global interconnects could be more problematic. As a result, the concern of increasing delay in the global wires may get worse with this additional temperature effect.

IV. Summary

In conclusion, a compact analytical thermal model has been presented to evaluate the spatial thermal distribution and the average interconnect temperature rise under the influence of vias. Both via effect and heat spreading have been taken into account to ensure accurate predictions. It has been shown that with the help of vias as efficient thermal paths, the effective thermal conductivity of the ILD materials can be significantly higher than their nominal values if via separation is comparable to the characteristic thermal length. Additionally, a closed form thermal model incorporating the via effect has been formulated to estimate the temperature rise of interconnects in multilevel metal arrays. It is shown that via effect must be considered in the thermal analysis of interconnect structures.

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